

REMARKS

Claims 16-35 are pending in the application. Claims 16-17, 20-21, 27-28, 31 and 24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Burgess (U.S. 4,642,160). Claims 16-17 and 31 are further rejected under 35 U.S.C. §103(a) as being unpatentable over Deroux-Dauphin, et al. (U.S. 4,964,212). Claims 16-17, 31 and 34 are yet further rejected under 35 U.S.C. §103(a) as being unpatentable over Foster, et al. (U.S. 5,108,553).

Applicants respectfully disagree and traverse each of the above-recited rejections. Applicants gratefully acknowledge the Examiner's indication of allowability of each of the other claims in the instant applications, namely Claims 18-19, 22-26 29-30, 32-33 and 35 if they were rewritten in independent form including all limitations of the base and intervening claims.

Claim 16 (and similarly claims 21 and 31) recites:

"forming a conductive circuit pattern on a first side of a dielectric layer, wherein the conductive circuit pattern includes a plurality of connection attachment terminals; and

laser-drilling a plurality of perforations from one side of the dielectric layer through to the

conductive circuit pattern to expose the connection attachment terminals."

Each of the cited references discloses laser-drilling holes to produce via holes that connects between circuit patterns and/or continuous metal layers when the via holes are filled with conductive material, and therefore the cited references do not make obvious the claimed invention.

Burgess, at Figure 6 and as referenced by the Examiner, discloses laser-drilling a via hole between a circuit layer of a multi-layer laminated dielectric circuit board structure and a metal foil layer and filling the via hole. However, such vias are not terminals in the sense of the present invention, and therefore applicants believe that it is improper to construe the "portion of the circuit layer whereat the conductive material connects the circuit pattern" as the terminals.

Further, the Examiner's assertion that if the teaching of Burgess were deficient as to terminals, then the terminals should be an equivalent of what is taught in Burgess is also improper, as in order to be an equivalent, the prior art structure must perform the same function in the same manner. Via connections, especially via connections to a ground plane do not perform the same function as the attachment terminals of the present invention. Further, applicants believe that the positions at which the vias are formed in Burgess are not and do not fulfill the function of terminals, as the vias disclosed in

Burgess are described as being formed between the inner conductor runs and the outer (foil) layer, as an interim process which later becomes a conductor run to conductor run via when the foil is subsequently etched (See Burgess col. 2 line 60 - col. 3, line 4).

For reasons similar to the reasons given above, Deroux-Dauphin also does not make obvious the claimed invention. Deroux-Dauphin describes making blind holes and through holes, but not laser-exposing conductive pattern terminals nor any equivalent.

Finally, Foster also does not make obvious the claimed invention, as Foster also only discloses the making of vias, which as pointed out above, are not terminals or their equivalent.

Therefore, for all of the reasons stated above, Applicants believe that the rejection under 35 U.S.C. §103(a) has been overcome.

CONCLUSION

In conclusion, Applicants respectfully submit that this Amendment, in view of the Remarks offered in conjunction therewith, are fully responsive to all aspects of the objections and rejections tendered by the Primary Examiner in the Office Action. Applicants respectfully submit that they have persuasively demonstrated that the above-identified Patent Application, including Claims 16-35 are in condition for allowance. Such action is earnestly solicited.

No fees should be incurred by this Amendment, but if there are any fees incurred by this Amendment, please deduct them from our Deposit Account No. 23-0830.

Respectfully submitted,



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